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Kind regards,

Team Nexperia

PEMIxCSP family

Integrated 4-, 6- and 8-channel passive filter network with ESD protection

Rev. 2 — 27 January 2012 Product data sheet

1. Product profile

1.1 General description

The devices are a family of 4-, 6- and 8-channel RC low pass filters which are designed to provide filtering of undesired RF signals on the I/O ports of portable communication or computing devices. In addition the devices incorporate diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages up to ±20 kV.

The PEMIxCSP family is fabricated using monolithic silicon technology and integrates up to eight resistors and 16 protection diodes in a single Wafer Level Chip-Size Package (WLCSP).

These features make the devices ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Integrated 4-, 6- and 8-channel π-type RC filter network
- Channel series resistance $R_{s(ch)}$ = 100 Ω
- Channel capacitance C_{ch} = 23 or 30 pF at $V_{bias(DC)}$ = 2.5 V
- Channel capacitance C_{ch} = 41 or 54 pF at $V_{bias(DC)}$ = 0 V
- Available in 10, 15 and 20-ball WLCSP
- ESD protection up to ±20 kV contact discharge according to IEC 61000-4-2, far exceeding level 4

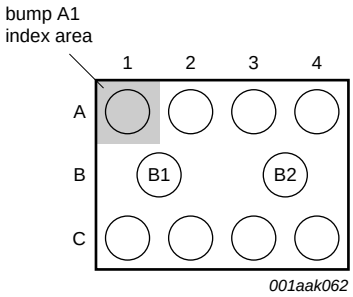
1.3 Applications

General-purpose ElectroMagnetic Interference (EMI) and Radio-Frequency Interference (RFI) filtering and downstream ESD protection for:

- Cellular phone and Personal Communication Systems (PCS) mobile handsets
- Cordless telephones
- Wireless data (WAN/LAN) systems

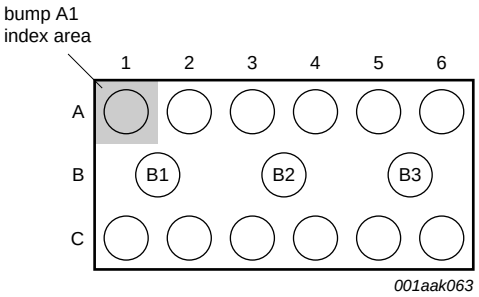
2. Pinning information

2.1 Pinning



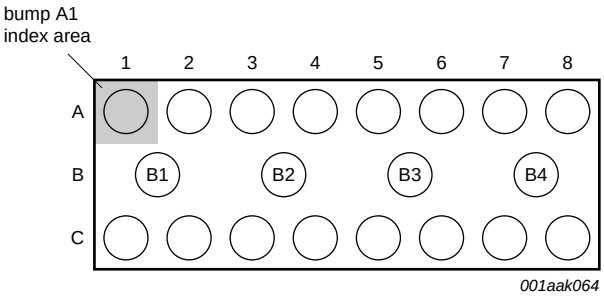
transparent top view,
solder balls facing down

Fig 1. PEMI4CSP: pin configuration



transparent top view,
solder balls facing down

Fig 2. PEMI6CSP: pin configuration



transparent top view,
solder balls facing down

Fig 3. PEMI8CSP: pin configuration

2.2 Pin description

Table 1. Pinning

Pin			Description
PEMI4CSP	PEMI6CSP	PEMI8CSP	
A1 and C1	A1 and C1	A1 and C1	filter channel 1
A2 and C2	A2 and C2	A2 and C2	filter channel 2
A3 and C3	A3 and C3	A3 and C3	filter channel 3
A4 and C4	A4 and C4	A4 and C4	filter channel 4
-	A5 and C5	A5 and C5	filter channel 5
-	A6 and C6	A6 and C6	filter channel 6
-	-	A7 and C7	filter channel 7
-	-	A8 and C8	filter channel 8
B1 and B2	B1, B2 and B3	B1, B2, B3 and B4	ground (GND)

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3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PEMI4CSP/RT	WLCSP10	wafer level chip-size package; 10 bumps; 1.56 × 1.05 × 0.61 mm	PEMI4CSP/RT
PEMI4CSP/RW	WLCSP10	wafer level chip-size package; 10 bumps; 1.56 × 1.05 × 0.61 mm	PEMI4CSP/RW
PEMI6CSP/RT	WLCSP15	wafer level chip-size package; 15 bumps; 2.36 × 1.05 × 0.61 mm	PEMI6CSP/RT
PEMI6CSP/RW	WLCSP15	wafer level chip-size package; 15 bumps; 2.36 × 1.05 × 0.61 mm	PEMI6CSP/RW
PEMI8CSP/RT/P	WLCSP20	wafer level chip-size package; 20 bumps; 3.16 × 1.05 × 0.61 mm	PEMI8CSP/RT/P
PEMI8CSP/RW/P	WLCSP20	wafer level chip-size package; 20 bumps; 3.16 × 1.05 × 0.61 mm	PEMI8CSP/RW/P

4. Functional diagram

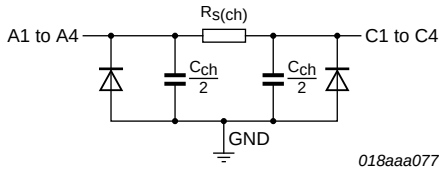


Fig 4. PEMI4CSP: schematic diagram

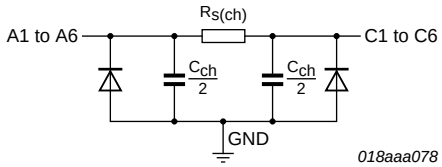


Fig 5. PEMI6CSP: schematic diagram

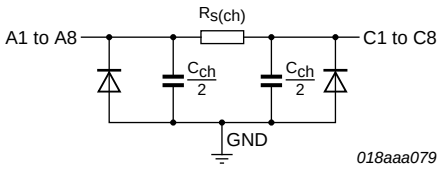


Fig 6. PEMI8CSP: schematic diagram

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5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+5.6	V
V_{ESD}	electrostatic discharge voltage	all pins to ground	[1]			
		contact discharge		-	±20	kV
		air discharge		-	±30	kV
		IEC 61000-4-2, level 4 all pins to ground				
		contact discharge		-	±8	kV
		air discharge		-	±15	kV
I_{ch}	channel current (DC)	T_{amb} = 70 °C		-	33	mA
P_{ch}	channel power dissipation	continuous power; T_{amb} = 70 °C		-	60	mW
P_{tot}	total power dissipation	continuous power; T_{amb} = 70 °C		-	250	mW
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance			80	100	120	Ω
C_{ch}	channel capacitance	for the total channel; f = 100 kHz	[1]				
	PEMIxCSP/RT	$V_{bias(DC)}$ = 0 V		33	41	49	pF
		$V_{bias(DC)}$ = 2.5 V		-	23	-	pF
	PEMIxCSP/RW	$V_{bias(DC)}$ = 0 V		43	54	65	pF
		$V_{bias(DC)}$ = 2.5 V		-	30	-	pF
V_{BR}	breakdown voltage	positive clamp; I_I = 1 mA		5.8	-	9	V
V_F	forward voltage	negative clamp; I_F = 1 mA		−1.5	-	−0.4	V
I_{LR}	reverse leakage current	per channel; V_I = 3.5 V		-	-	0.1	µA
R_{dyn}	dynamic resistance	I = 1 A	[2]				
		positive transient		-	0.3	-	Ω
		negative transient		-	0.85	-	Ω

[1] Guaranteed by design.

[2] According to IEC 61000-4-5 and IEC 61000-4-9.

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Table 5. Frequency characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{il}	insertion loss	R_{source} = 50 Ω; R_L = 50 Ω				
	PEMIxCSP/RT	800 MHz < f_i < 3 GHz	25	30	-	dB
		f_i = 1.7 GHz	-	35	-	dB
	PEMIxCSP/RW	800 MHz < f_i < 3 GHz	27	32	-	dB
		f_i = 1.7 GHz	-	37	-	dB
α_{ct}	crosstalk attenuation	R_{source} = 50 Ω; R_L = 50 Ω; 800 MHz < f_i < 3 GHz	-	30	-	dB
f_{-3dB}	cut-off frequency	R_{source} = 50 Ω; R_L = 50 Ω				
	PEMIxCSP/RT		-	128	-	MHz
	PEMIxCSP/RW		-	98	-	MHz

7. Application information

7.1 Insertion loss

The devices are designed as EMI/RFI filters for multichannel interfaces.

All measurements were performed in a typical 50 Ω NetWork Analyzer (NWA) setup as shown in Figure 7. The measured insertion loss in a 50 Ω system is depicted in Figure 8.

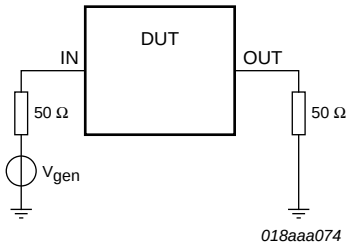
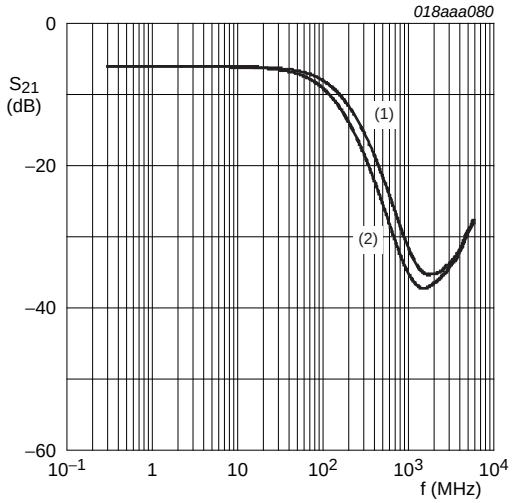


Fig 7. Frequency response setup

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(1) PEMIxCSP/RT

(2) PEMIxCSP/RW

Fig 8. Frequency response curves

7.2 Use cases

The selection of one of the filter device has to be performed in dependence of the maximum clock frequency, the driver strength, the capacitive load of the sink and the maximum applicable rise and fall times.

7.3 LCD interfaces, medium-speed interfaces

For digital interfaces such as Liquid Crystal Display (LCD) interfaces running at clock speeds between 10 MHz and 25 MHz or more, the devices can be used in dependence of the sink load, the clock speed, the driver strength and the rise and fall time requirements. The minimum EMI filter requirements may be an important factor, too.

7.4 Keypad, low-speed interfaces

Especially for lower-speed interfaces such as keypads, low-speed serial interfaces and low-speed control signals, the PEMIxCSP family offers a very robust ESD protection and strong suppression of unwanted frequencies (EMI filtering). Due to their small size the devices can easily be spread on a Printed-Circuit Board (PCB) in order to move the ESD and EMI protection close to the part of the design which shall be protected.

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8. Marking

All dies are laser-marked with the following information (see Figure 9 and 10):

- A marker indicating the pin A1 position.
- Two lines of characters or numbers:
  - The first line (placeholder <marking code>) indicates the marking code. Mapping of product type numbers to marking codes is given in Table 6.
  - The second line (placeholder <lot ID>) indicates the production lot. This information enable to track a device down to a particular production date.

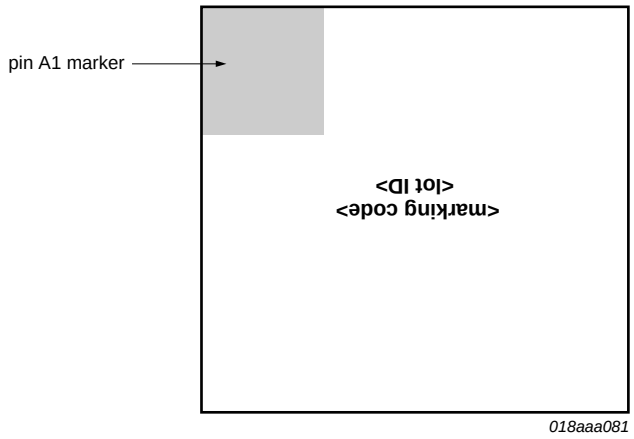


Fig 9. PEMI4CSP and PEMI6CSP: outline of the marking

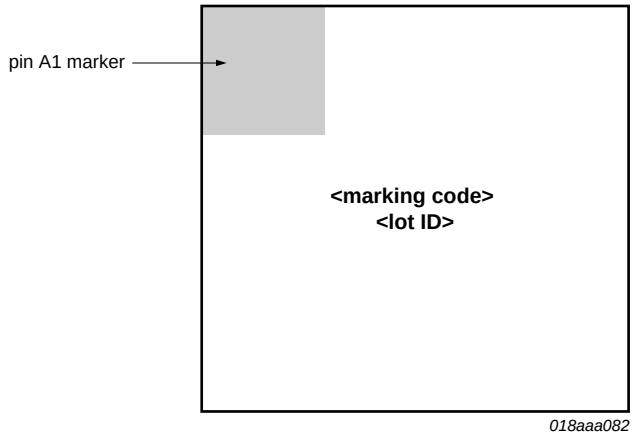


Fig 10. PEMI8CSP: outline of the marking

Table 6. Marking codes

Type number	Marking code	Type number	Marking code
PEMI4CSP/RT	RT	PEMI6CSP/RW	RW
PEMI4CSP/RW	RW	PEMI8CSP/RT/P	RT
PEMI6CSP/RT	RT	PEMI8CSP/RW/P	RW

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9. Package outline

WLCSP10: wafer level chip-size package; 10 bumps (4-2-4)

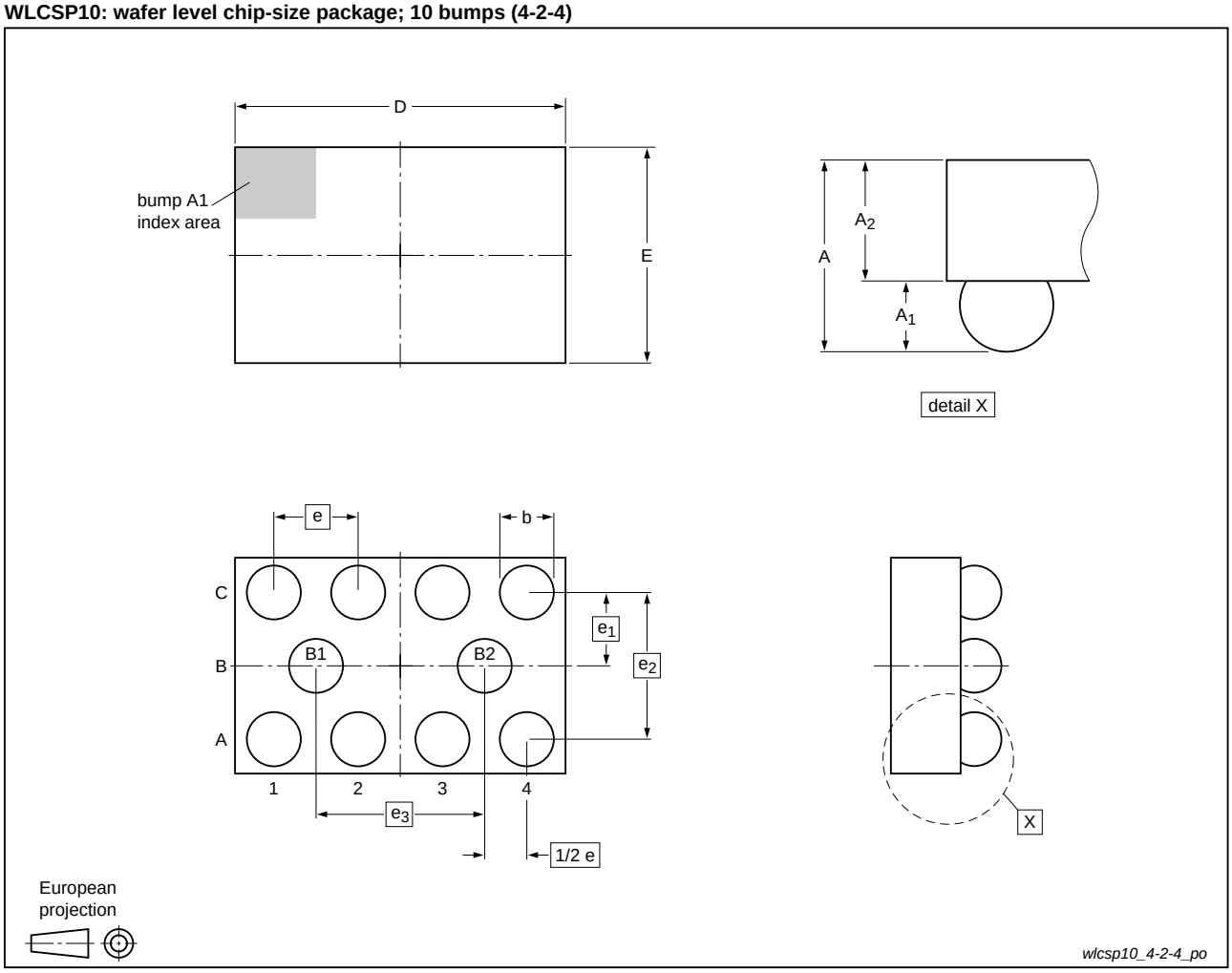


Fig 11. Package outline PEMI4CSP (WLCSP10)

Table 7. Package outline dimensions of PEMI4CSP

Symbol	Min	Typ	Max	Unit
A	0.57	0.61	0.65	mm
A_1	0.18	0.20	0.22	mm
A_2	0.39	0.41	0.43	mm
b	0.21	0.26	0.31	mm
D	1.51	1.56	1.61	mm
E	1.00	1.05	1.10	mm
e	-	0.4	-	mm
e_1	-	0.346	-	mm
e_2	-	0.692	-	mm
e_3	-	0.8	-	mm

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WLCSP15: wafer level chip-size package; 15 bumps (6-3-6)

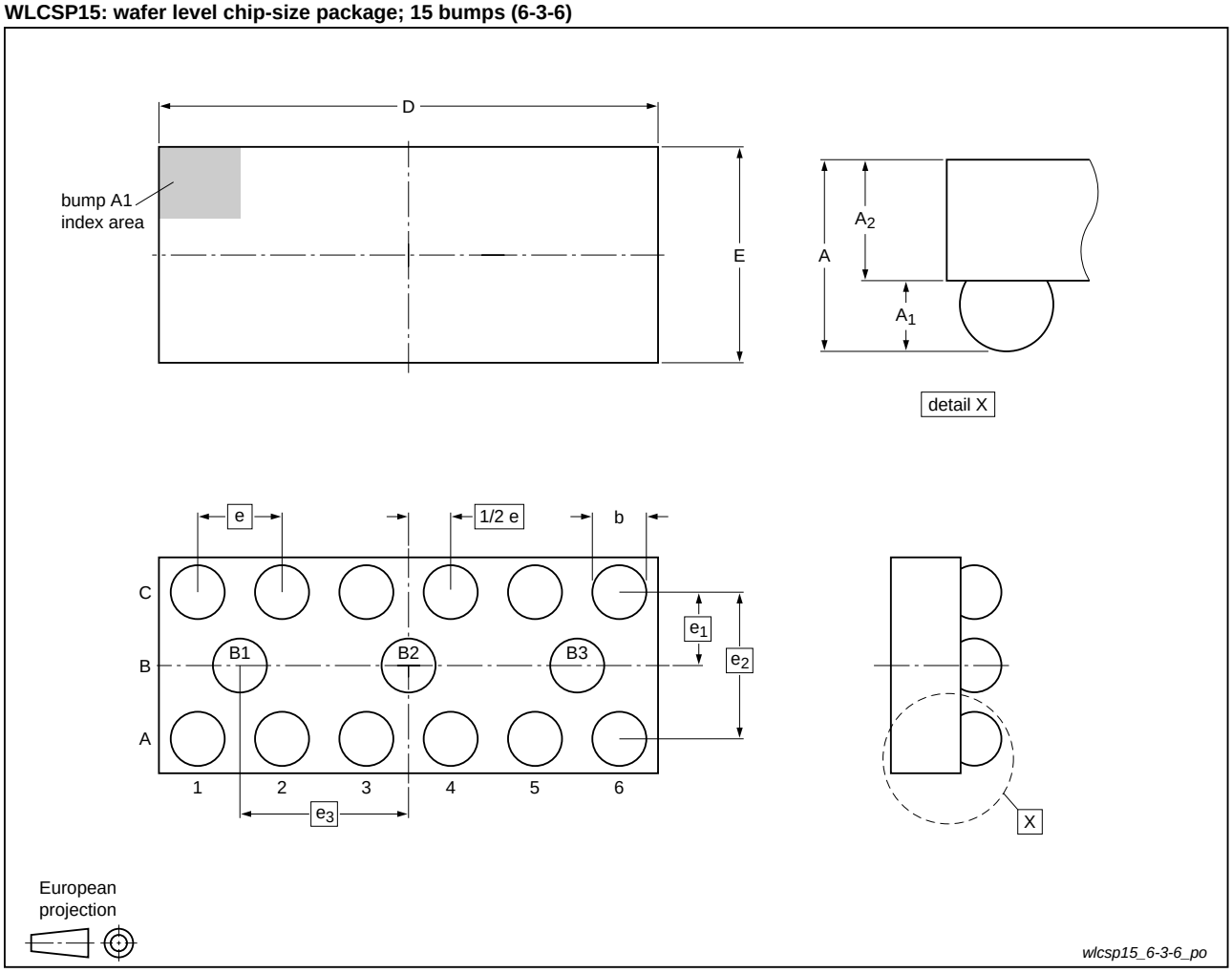


Fig 12. Package outline PEMI6CSP (WLCSP15)

Table 8. Package outline dimensions of PEMI6CSP

Symbol	Min	Typ	Max	Unit
A	0.57	0.61	0.65	mm
A_1	0.18	0.20	0.22	mm
A_2	0.39	0.41	0.43	mm
b	0.21	0.26	0.31	mm
D	2.31	2.36	2.41	mm
E	1.00	1.05	1.10	mm
e	-	0.4	-	mm
e_1	-	0.346	-	mm
e_2	-	0.692	-	mm
e_3	-	0.8	-	mm

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WLCSP20: wafer level chip-size package; 20 bumps (8-4-8)

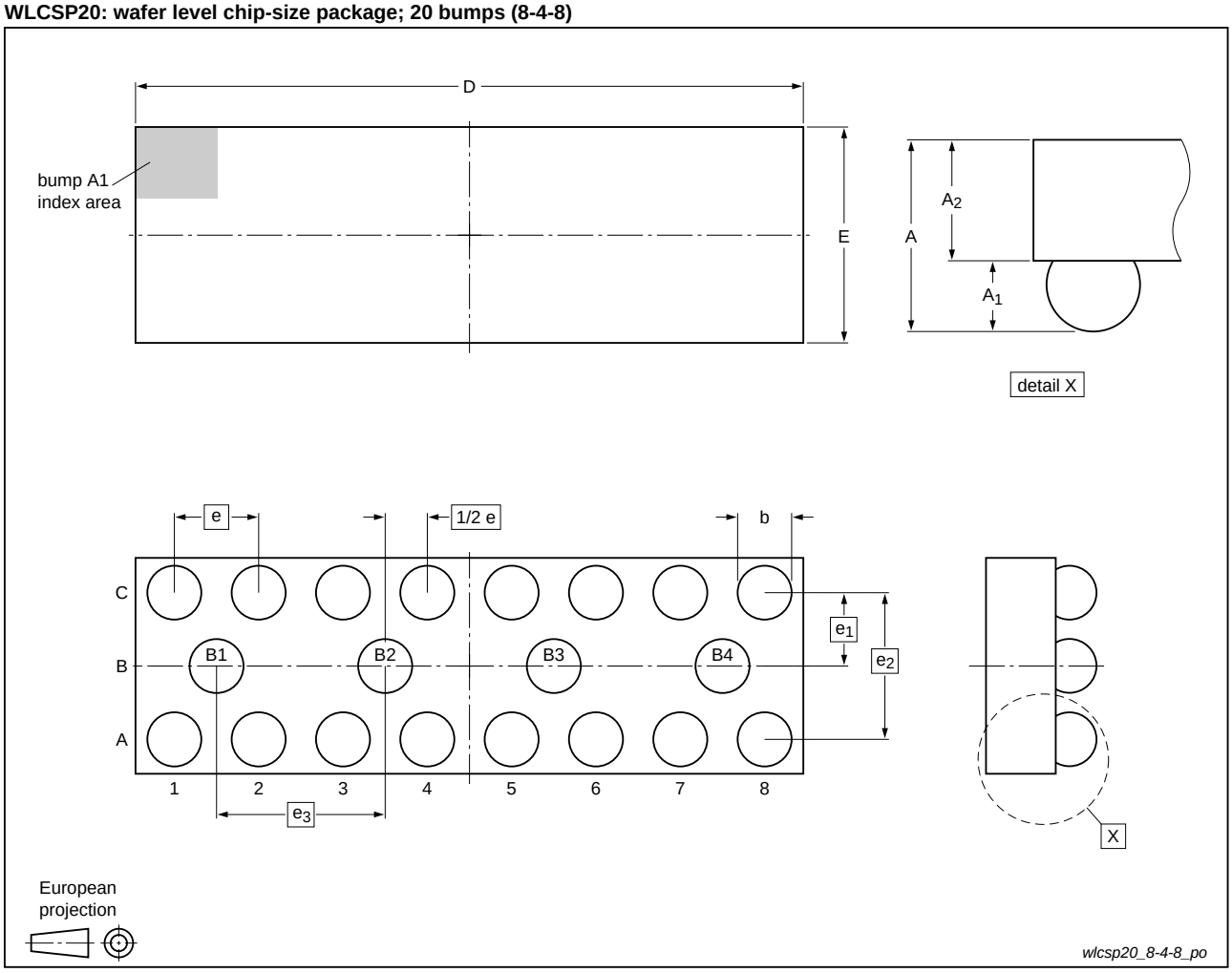


Fig 13. Package outline PEMI8CSP (WLCSP20)

Table 9. Package outline dimensions of PEMI8CSP

Symbol	Min	Typ	Max	Unit
A	0.57	0.61	0.65	mm
A_1	0.18	0.20	0.22	mm
A_2	0.39	0.41	0.43	mm
b	0.21	0.26	0.31	mm
D	3.11	3.16	3.21	mm
E	1.00	1.05	1.10	mm
e	-	0.4	-	mm
e_1	-	0.346	-	mm
e_2	-	0.692	-	mm
e_3	-	0.8	-	mm

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10. Design and assembly recommendations

10.1 PCB design guidelines

It is recommended, for optimum performance, to use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. Refer to Table 10 for the recommended Printed-Circuit Board (PCB) design parameters.

Table 10. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	250 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	325 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

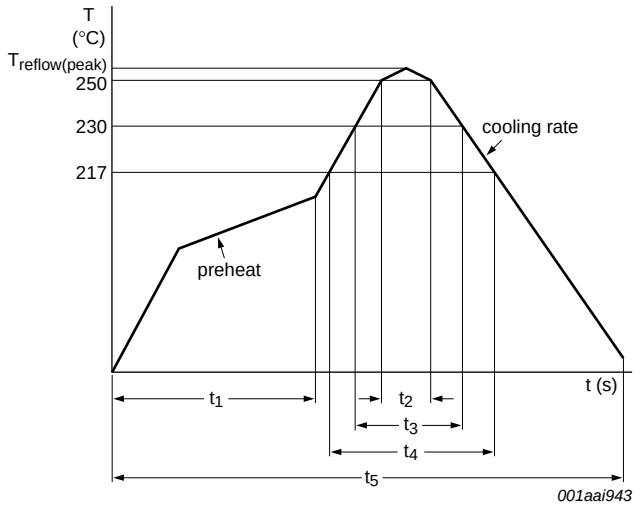
10.2 PCB assembly guidelines for Pb-free soldering

Table 11. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	290 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %) Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 14

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The device is capable of withstanding at least three reflows of this profile.

Fig 14. Pb-free solder reflow profile

Table 12. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		pre-heat	2.5	-	4.0	°C/s

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11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMIXCSP_FAM v.2	20120127	Product data sheet	-	PEMIXCSP_FAM v.1
PEMIXCSP_FAM v.1	20110203	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 27 January 2012
Document identifier: PEMIXCSP_FAM